REMARKS/ARGUMENT

Claims 1-38 are pending in the present application. Claims 39-57 were withdrawn in response to a restriction requirement. The Examiner correct identifies that claims 1-38 are pending in paragraph 1 of the Office Action, but, just for clarification, other portions of the Office Action incorrectly indicate claims 1-37 are pending. Claim 38 is a claim dependent on claim 37 and has not been withdrawn by applicants.

Claim Objection

The Examiner has objected to terminology in claim 1 reciting that "a second standard scan cell positioned immediately after the combinational test point". This language would be understood by one of ordinary skill in the art to mean that a "combinational test point" has been inserted into the scan path of a logic circuit which uses scan-based delay testing. In other words, the "combinational test point" is positioned in a "scan chain" so as to be positioned immediately after a "first standard scan cell" in the scan chain so that a "second standard scan cell" in the scan chain is positioned immediately after the "combinational test point". An example of this is illustrated in FIG. 2(b) which shows a combinational gate inserted between the scan cells D_1 and D_2. As depicted in FIG. 2(b), the combinational test point is positioned immediately after D_1 while the scan cell D_2 is "positioned immediately after the combinational test point".

The Examiner has object to terminology in claim 16 which refers to an "untestable transition delay fault". This terminology would be understood by one of ordinary skill in the art to mean a fault which would not be testable under the transition delay fault model. In other words, the delay fault coverage would not be sufficient to allow the system to detect the particular fault using the transition delay fault model. Consider, for example, the discussion at pages 5-8 of the Specification which discusses many aspects of delay fault coverage in the prior art.

Claim Rejections

The Examiner has rejected claims 1-37 under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent No. 6,148,425 to Bhawmik et al. (herein the "Bhawmik patent"). Applicants respectfully traverse.

The Bhawmik patent is directed to a scan-based built-in self-test (BIST) architecture for detecting path-delay faults. See Abstract. The Bhawmik patent attempts to improve fault coverage for detecting path-delay faults in a sequential circuit by inserting observation points in the circuit under test (CUT). The observation points are selected by performing path-delay fault testing for each path in a set of paths in the sequential circuit. See Col. 2, lines 40-54. The Bhawmik patent discloses that the prior art already teaches similar improved path-delay fault testing techniques for combinational circuits. See Col. 2, lines 27-39. The Bhawmik patent extends such prior art techniques to sequential circuits by converting the sequential circuit into a combinational circuit or into a less complex sequential circuit which includes a combinational portion and a plurality of can flip-flops. See Col. 3, lines 15-20.

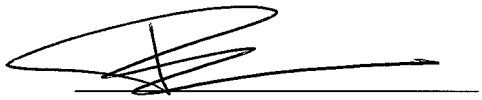
Accordingly, as discussed therein, the Bhawmik patent, like the prior art discussed in the Bhawmik patent, is directed to inserting test points directly into the circuit, thereby altering the circuit topology. In other words, the Bhawmik patent is directed to traditional test point insertion techniques in which test points are inserted into functional paths. In the present invention, on the other hand, the test points are not inserted into the functional path but instead are "inserted into the scan path". Specification at page 19, [paragraph 80]. In other words, as recited in the claim, a "combinational test point is positioned immediately after" a "first standard scan cell" in a "scan chain" with a "second standard scan cell positioned immediately after" the combinational test point in the scan chain. The sections in the Bhawmik patent cited by the Examiner do not disclose these claims limitations. Rather, these sections of the Bhawmik patent discuss the difference between a sequential and combinational circuit and how a sequential circuit can be converted into a partial or full-scan-based design. Again, the Bhawmik patent does not disclose inserting the combinational test points into a scan chain. The same can be said of all of the claims pending, since all of the claims contain similar language regarding the nature of the invention.

Moreover, with regard to claim 2 and 12, the Bhawmik patent does not disclose positioning the combinational test point in the scan chain so as "to prevent shift dependency between the first standard scan cell and the second standard scan cell."

With regard to claim 16, the Bhawmik patent categorically does not disclose anything with regard to "transition delay faults". It should be noted that the Bhawmik patent is specifically limited to the context of the path delay fault model, which as noted in the Speficiation at page 5, is completely different from the transition delay fault model.

Applicants respectfully submit that the pending claims represent patentable subject matter and that the application is in condition for allowance. If the Examiner has any questions, please feel free to contact the undersigned at 609 951-2522. Authorization is hereby given to charge any fees which may be required, except the issue fee, to Deposit Account 14-0627.

Respectfully submitted,



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